Sunpyo Hong

CONTACT INFORMATION

Technology Pathfinding and Innovations [SSG/DPD/TPI]

Intel Corporation
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RESEARCH INTERESTS

My general research interest is on energy-efficient computer architecture. I focus on discovering insights into performance and power by application-driven architectural modeling, real experiments, and simulations. These insights lead to finding bottlenecks in architecture and software stack, and further lead to more energy-efficient system implementation.

EDUCATION

Georgia Institute of Technology, Atlanta, Georgia

Ph.D., Electrical and Computer Engineering, May 2008 - Dec 2012

- Thesis: *Modeling Performance and Power for Energy-Efficient Computing*
- Adviser: Professor Hyesoon Kim
- Area of Study: Computer Architecture, Energy Analysis, Software Engineering

M.S.ECE, Electrical and Computer Engineering, May - Dec 2002, Jan 2007 - Apr 2008

- Specialization in Computer Architecture, Coursework Completion Option

B.S., Electrical and Computer Engineering, May, 1998 - Apr, 2002

- Cumulative GPA : 3.86 / 4.00 [Highest-Honor Criteria: 3.55]
- Specialization in Digital Signal Processing [DSP]

EMPLOYMENT HISTORY

Intel Corporation, SSG/DPD/TPI, Hudson, MA — Dec 2012 - Present
Software Engineer

Georgia Institute of Technology, Atlanta, GA — Jan 2007 - Dec 2012
Graduate Research Assistant

Intel Corporation, SSG/DPD/TPI, Hudson, MA — Sept 2010 - Apr 2011
Graduate Technical Intern

Hanbit Electronics, Suwon, Korea — Dec 2003 - Nov 2006
Hardware Engineer

PUBLICATIONS

[**ISCA'09**] Sunpyo Hong, Hyesoon Kim, *"A Memory-level and Thread-level Parallelism Aware GPU Architecture Performance Analytical Model"*, in Proceedings of the 36th Annual International Symposium on Computer Architecture, Austin, Texas, USA, June 2009. ***[Citations]:*** 40 in ACM, 161 in Google Scholar.

[**ISCA'10**] Sunpyo Hong, Hyesoon Kim, *"An Integrated GPU Power and Performance Model"*, in Proceedings of the 37th Annual International Symposium on Computer Architecture, Saint-Malo, France, June 2010. ***[Citations]:*** 22 in ACM, 124 in Google Scholar.

[**MICRO'09**] Chi-Keung Luk, Sunpyo Hong, Hyesoon Kim, *"Qilin: Exploiting Parallelism on Heterogeneous Multiprocessors with Adaptive Mapping"*, in Proceedings of the 42nd Annual International Symposium on Microarchitecture, New York, USA. ***[Citations]:*** 45 in ACM, 11 in IEEE, 124 in Google Scholar.

Submitted Publication

Sunpyo Hong, Aniruddha Dasgupta, Hyesoon Kim, Jinil Park, *"A New Fine-Scaled Thermal-Analysis System For GPU Architectures using Thermocouples"*, Submitted to IEEE TCAS2, 2012.

Sunpyo Hong, Joo Hwan Lee, Hyesoon Kim *"An OpenCL Throughput Model for Energy-Efficient and High-Performance Work Partitioning"*, Submitted to ISCA, 2013.

Research and Professional Experiences

Intel Corporation, SSG/DPD/TPI, Hudson, MA,

Software Engineer **Dec 2012 - Present**

- Research and advanced development for Intel software and architecture tools
- Working on GT-PIN instrumentation system for Intel GPUs
- Energy efficiency analysis using performance and power predictions
- Focuses on parallel programming, many-core architecture, and prototyping tools
- Supervisors: Dr. Chi-keung Luk, Dr. Peng Tu [Manager], Dr. Geoff Lowney [Intel Fellow]

Georgia Institute of Technology, Atlanta, GA

Graduate Research Assistant for Prof. Hyesoon Kim **Jan 2007 - Dec 2012**

Performance Modeling

- Published the first analytical model for GPU architecture in [**ISCA'09**]
- Propose the model for performance analysis using essential architectural features
- Analyze the effect of instruction mixture, threads, and memory-access patterns
- Devise benchmarks that produce different performances and memory patterns
- Provide an insight on performance and a mechanism to visualize bottlenecks
- Research on extending the work to general many-core architecture using OpenCL

Power Modeling

- Developed power, temperature models and integrated with the performance work
- Predict an optimum number of cores by leveraging the proposed models
- Investigate the effect of increased temperature on energy consumption
- Published this work in [**ISCA'10**]

Workload Scheduling

- Focused on the problem that heterogeneous execution is energy efficient
- Developed the software framework, Qilin, that dynamically determines a workload distribution ratio between CPU and GPU
- Published the work in [**MICRO'09**] as a co-author
- Investigate further using OpenCL on multiple heterogeneous architectures

Intel Corporation, SSG/DPD/TPI, Hudson, MA,

Graduate Technical Intern **Sept 2010 - Apr 2011**

- Analyze the MIC architecture using micro benchmarks and the analytical model
- Determine the upper-bound and lower-bound of potential application performances
- Developed the bottom-up approach to understand microarchitecture considering threading, vectorization, and cache and memory effects in real experiment
- Manager: Dr. Chi-keung Luk

Hanbit Electronics, Suwon, Korea

Hardware Engineer **Dec 2003 - Nov 2006**

- Fulfilled the Korean military duty from the work completion
- Developed products with Samsung, which integrate and control home appliances
- Designed circuits for LCD-control board, USB drive, and CFC card

Certificates

Government-Accredited Certificates

- Certificates needed to work in Hanbit Electronics
- Fulfilled the mandatory Korean military requirement from the work completion
- Engineer information processing certificate [No. 03201101061Y]
- Engineer radio telecommunication equipment certificate [No. 03201100252Z]
- Preparation dates : Feb 2003 - Oct 2003

Professional Activities

Invited Journal Reviewer

- Transactions on Parallel and Distributed Systems (TPDS), IEEE, 2013
- Journal of Parallel and Distributed Computing (JPDC), Elsevier, 2011

External Reviewer

- Computer Architecture (ISCA), 2010, 2011
- Microarchitecture (MICRO), 2011
- Workload Characterization (IISWC), 2009
- High Performance Computer Architecture (HPCA), 2010
- Parallel Architectures and Compilation Techniques (PACT), 2010

Membership

- Student Member of IEEE, since 2009
- Student Member of ACM and SIGARCH, since 2009

Technical Skills

Computer Programming and Scripting Languages

- Expert in C/C++, CUDA, OpenCL, Python, LLVM, Profiling
- OpenMP, OpenGL, PIN, CilkPlus, TBB, PThreads, DirectX
- Matlab: Signal processing, Linear algebra, Visualization

Electrical Engineering

- Power tools and simulations
- Setting up power measurements, oscilloscope, multimeter
- Digital circuits, Debugging HW circuit boards using wires and soldering

Awards

Georgia Institute of Technology

- Faculty Honors (GPA of 4.00)
- Dean's Lists (GPA of 3.00 or above)

Activities and Background

UROP, Undergraduate Research in Georgia Tech

- Participated in UROP program for selected undergraduate students
- Multifractal analysis for signal processing under Prof. David Anderson, Fall 2001
- Modeling an unknown system in noisy environment under Prof. Verriest, Spring 2001
- Participated as a selected tutor among graduate students to teach ECE classes

Other Activities and Information

- Citizen of Republic of Korea
- Graduate Teaching Assistant for ECE2025 (Digital Signal Processing), Fall 2002
- Honor Societies: Tau Beta Phi, Eta Kappa Nu, Gamma Beta Phi, Golden Key, NSCS
- Fluency in English and Korean. Learning Chinese.